BARIŞ ARSLAN
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Ögrenim Bilgisi

Doktora 2003 - 2013	University of California, San Diego, Jacobs School of Engineering , Computer Science and Engineering, Amerika Birleşik Devletleri
Yüksek Lisans 2000 - 2002	University of California, San Diego, Jacobs School of Engineering, Computer Science and Engineering, Amerika Birleşik Devletleri
Lisans 1996 - 2000	İhsan Doğramacı Bilkent Üniversitesi, Mühendislik Fakültesi, Bilgisayar Mühendisliği Bölümü, Türkiye

Yabancı Diller

İngilizce, C2 Ustalık

Yaptığı Tezler

Doktora, Adaptive Test Cost And Quality Optimization Through An Effective Yet Efficient Delivery Of Chip Specific Tests, University of California, San Diego, Jacobs School of Engineering, Computer Science and Engineering, 2013

Akademik Unvanlar / Görevler

Dr.Öğr.Üyesi 2021 - Devam Ediyor	Acıbadem Mehmet Ali Aydınlar Üniversitesi, Mühendislik ve Doğa Bilimleri Fakültesi, Bilgisayar Mühendisliği Bölümü

Desteklenen Projeler

1. Arslan B., TÜBİTAK Projesi, Gerçek Zamanlı Test Veri Analizi ile Test Optimizasyonu, 2018 - 2022
2. Arslan B., TÜBİTAK Projesi, Entegre Devre Zamanlamasını etkileten Küçük Boyutlu Üretim Hatalarının Tanılanması, 2015 - 2017

SCI, SSCI ve AHCI İndekslerine Giren Dergilerde Yayınlanan Makaleler

1. **Aggressive Test Cost Reductions Through Continuous Test Effectiveness Assessment**
   Arslan B., Orailoglu A.
   IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, cilt.35, sa.12, ss.2093-2103, 2016 (SCI-Expanded)
2. **Power-Aware Delay Test Quality Optimization for Multiple Frequency Domains**

Arslan B., Orailoglu A.
IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, cilt.35, sa.1, ss.141-154, 2016 (SCI-Expanded)

Hakemli Kongre / Sempozyum Bildiri Kitaplarında Yer Alan Yayınlar

1. **Test Cost-Test Quality Modeling For Adaptive Test**
   Demiray B. Z., Arslan B.
   2022 IEEE INTERNATIONAL CONFERENCE ON AUTOMATION, QUALITY AND TESTING, ROBOTICS (AQTR), Cluj-Napoca, Romanya, 19 - 21 Mayıs 2022, ss.1-6
2. **Small Delay Defect Diagnosis through Failure Observation Ordering**
   ARSLAN B.
   PROCEEDING OF 2016 IEEE INTERNATIONAL CONFERENCE ON AUTOMATION, QUALITY AND TESTING, ROBOTICS (AQTR), Cluj-Napoca, Romanya, 19 - 21 Mayıs 2016, ss.67-72
3. **Tracing the Best Test Mix through Multi-Variate Quality Tracking**
   Arslan B., Orailoglu A.
   IEEE 31st VLSI Test Symposium (VTS), California, Amerika Birleşik Devletleri, 29 Nisan - 02 Mayıs 2013
4. **Full Exploitation of Process Variation Space for Continuous Delivery of Optimal Delay Test Quality**
   Arslan B., Orailoglu A.
   18th Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japonya, 22 - 25 Ocak 2013, ss.552-557
5. **Delay Test Resource Allocation and Scheduling for Multiple Frequency Domains**
   Arslan B., Orailoglu A.
   30th IEEE VLSI Test Symposium (VTS), Hawaii, Amerika Birleşik Devletleri, 23 - 25 Nisan 2012, ss.114-119
6. **Adaptive Test Optimization through Real Time Learning of Test Effectiveness**
   Arslan B., Orailoglu A.
   Design, Automation and Test in Europe Conference (DATE), Grenoble, Fransa, 14 - 18 Mart 2011, ss.1430-1435
7. **Adaptive Test Framework for Achieving Target Test Quality at Minimal Cost**
   Arslan B., Orailoglu A.
   20th Asian Test Symposium (ATS), New Delhi, Hindistan, 20 - 23 Kasım 2011, ss.323-328
8. **Delay Test Quality Maximization through Process-aware Selection of Test Set Size**
   Arslan B., Orailoglu A.
   IEEE International Conference on Computer Design, Amsterdam, Hollanda, 3 - 06 Ekim 2010, ss.390-395
9. **Test cost reduction through a reconfigurable scan architecture**
   Arslan B., Orailoglu A.
   35th International Test Conference, Charlottetown, Kanada, 26 - 28 Ekim 2004, ss.945-952
10. **CircularScan: A scan architecture for test cost reduction**
    Arslan B., Orailoglu A.
    Design, Automation and Test in Europe Conference and Exhibition (DATE 04), Paris, Fransa, 16 - 20 Şubat 2004, ss.1290-1295
11. **Extending the applicability of parallel-serial scan designs**
    Arslan B., Sinanoglu O., Orailoglu A.
    IEEE International Conference on Computer Design, San-Jose, Kostarika, 11 - 13 Ekim 2004, ss.200-203
12. **Design space exploration for aggressive test cost reduction in circular scan Architectures**
    Arslan B., Orailoglu A.
    International Conference on Computer Aided Design (ICCAD 2004), San-Jose, Kostarika, 7 - 11 Kasım 2004, ss.726-731
13. **Extracting precise diagnosis of bridging faults from stuck-at fault information**
    Arslan B., Orailoglu A.
    12th Asian Test Symposium, Xian, Çin, 16 - 19 Kasım 2003, ss.230-235

14. **Fault dictionary size reduction through test response superposition**
Arslan B., Orailoglu A.
20th IEEE International Conference on Computer Design, Freiburg, Almanya, 16 - 18 Eylül 2002, ss.480-485

Akademik İdari Deneyim

2018 - 2021	**Anabilim/Bilim Dalı Başkanı**	İstanbul Şehir Üniversitesi, Fen Bilimleri Enstitüsü, Electrical and Computer Engineering Department

Metrikler

Yayın: 17
Atıf (WoS): 85
Atıf (Scopus): 103
H-İndeks (WoS): 4
H-İndeks (Scopus): 5

Araştırma Alanları

Bilgisayar Bilimleri, Yapay Zeka, Bilgisayarda Öğrenme ve Örüntü Tanıma

Akademi Dışı Deneyim

Şirket, OakNorth, Data Science
Şirket, QUALCOMM INC., QCT
Şirket, Marvell Technology, Inc., Engineering
Marvell Semiconductor Inc.
Şirket, Intel Corporation, Engineering
Intel Corporation