

Asst. Prof. BARIŞ ARSLAN

Personal Information

Email: Baris.Arslan@acibadem.edu.tr

Web: <https://avesis.acibadem.edu.tr/Baris.Arslan>

Education Information

Doctorate, University of California, San Diego, Computer Science, United States Of America 2000 - 2013

Post Graduate, University of California, San Diego, Computer Science, United States Of America 2000 - 2002

Under Graduate, Ihsan Dogramaci Bilkent University, Faculty Of Engineering, Department Of Computer Engineering, Turkey 1996 - 2000

Foreign Languages

English, C2 Mastery

Research Areas

Artificial Intelligence, Computer Learning and Pattern Recognition

Academic Titles / Tasks

Assistant Professor, Acibadem Mehmet Ali Aydinlar University, Faculty of Engineering, Computer Science, 2021 - Continues

Assistant Professor, Istanbul Sehir University, Faculty Of Engineering And Natural Sciences, Department Of Computer Engineering, 2014 - 2020

Academic and Administrative Experience

Head of Department, Istanbul Sehir University, Institute Of Science, Electrical and Computer Engineering, 2018 - 2020

Courses

Big Data Analysis, Post Graduate, 2014 - 2015, 2015 - 2016, 2016 - 2017, 2017 - 2018, 2018 - 2019, 2019 - 2020

Exploratory Data Analysis, Under Graduate, 2018 - 2019, 2019 - 2020

Machine Learning, Post Graduate, 2018 - 2019, 2019 - 2020

Machine Learning, Under Graduate, 2018 - 2019, 2019 - 2020

Computer Architecture, Under Graduate, 2014 - 2015, 2015 - 2016, 2016 - 2017, 2017 - 2018, 2018 - 2019, 2019 - 2020

Advanced Algorithms, Under Graduate, 2014 - 2015, 2015 - 2016, 2016 - 2017, 2017 - 2018

Data Visualization, Under Graduate, 2014 - 2015, 2015 - 2016, 2016 - 2017

Data Visualization, Post Graduate, 2014 - 2015, 2015 - 2016, 2016 - 2017

Articles Published in Journals That Entered SCI, SSCI and AHCI Indexes

- I. **Aggressive Test Cost Reductions Through Continuous Test Effectiveness Assessment**
Arslan B., Orailoglu A.
IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol.35, no.12, pp.2093-2103, 2016 (Journal Indexed in SCI)
- II. **Power-Aware Delay Test Quality Optimization for Multiple Frequency Domains**
Arslan B., Orailoglu A.
IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol.35, no.1, pp.141-154, 2016 (Journal Indexed in SCI)

Refereed Congress / Symposium Publications in Proceedings

- I. **Small Delay Defect Diagnosis through Failure Observation Ordering**
ARSLAN B.
PROCEEDING OF 2016 IEEE INTERNATIONAL CONFERENCE ON AUTOMATION, QUALITY AND TESTING, ROBOTICS (AQTR), Cluj-Napoca, Romania, 19 - 21 May 2016, pp.67-72
- II. **Tracing the Best Test Mix through Multi-Variate Quality Tracking**
Arslan B., Orailoglu A.
IEEE 31st VLSI Test Symposium (VTS), California, United States Of America, 29 April - 02 May 2013
- III. **Full Exploitation of Process Variation Space for Continuous Delivery of Optimal Delay Test Quality**
Arslan B., Orailoglu A.
18th Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, 22 - 25 January 2013, pp.552-557
- IV. **Delay Test Resource Allocation and Scheduling for Multiple Frequency Domains**
Arslan B., Orailoglu A.
30th IEEE VLSI Test Symposium (VTS), Hawaii, United States Of America, 23 - 25 April 2012, pp.114-119
- V. **Adaptive Test Framework for Achieving Target Test Quality at Minimal Cost**
Arslan B., Orailoglu A.
20th Asian Test Symposium (ATS), New Delhi, India, 20 - 23 November 2011, pp.323-328
- VI. **Adaptive Test Optimization through Real Time Learning of Test Effectiveness**
Arslan B., Orailoglu A.
Design, Automation and Test in Europe Conference (DATE), Grenoble, France, 14 - 18 March 2011, pp.1430-1435
- VII. **Delay Test Quality Maximization through Process-aware Selection of Test Set Size**
Arslan B., Orailoglu A.
IEEE International Conference on Computer Design, Amsterdam, Netherlands, 3 - 06 October 2010, pp.390-395
- VIII. **Test cost reduction through a reconfigurable scan architecture**
Arslan B., Orailoglu A.
35th International Test Conference, Charlottetown, Canada, 26 - 28 October 2004, pp.945-952
- IX. **Extending the applicability of parallel-serial scan designs**
Arslan B., Sinanoglu O., Orailoglu A.
IEEE International Conference on Computer Design, San-Jose, Costa Rica, 11 - 13 October 2004, pp.200-203
- X. **CircularScan: A scan architecture for test cost reduction**
Arslan B., Orailoglu A.
Design, Automation and Test in Europe Conference and Exhibition (DATE 04), Paris, France, 16 - 20 February 2004, pp.1290-1295
- XI. **Design space exploration for aggressive test cost reduction in circular scan Architectures**
Arslan B., Orailoglu A.
International Conference on Computer Aided Design (ICCAD 2004), San-Jose, Costa Rica, 7 - 11 November 2004, pp.726-731

XII. Extracting precise diagnosis of bridging faults from stuck-at fault information

Arslan B., Orailoglu A.

12th Asian Test Symposium, Xian, China, 16 - 19 November 2003, pp.230-235

XIII. Fault dictionary size reduction through test response superposition

Arslan B., Orailoglu A.

20th IEEE International Conference on Computer Design, Freiburg, Germany, 16 - 18 September 2002, pp.480-485

Supported Projects

Arslan B., TUBITAK Project, Gerçek Zamanlı Test Veri Analizi ile Test Optimizasyonu, 2018 - 2021

Citations

Total Citations (WOS):84

h-index (WOS):4

Non Academic Experience

Company, OakNorth, -

Company, Qualcomm Inc., QCT

Company, Marvell Semiconductor Inc., -

Company, Intel Corporation, -